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PATENT & TRADEMARK OFFICE

Attorney Docket No. 1614.1082

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Hideo MIYAKE et al.

Application No.:

Group Art Unit:

Examiner:

Filed: September 28, 2000

For: METHOD OF CONTROLLING A CACHE MEMORY TO INCREASE AN ACCESS SPEED TO A MAIN MEMORY, AND A COMPUTER USING THE METHOD

INFORMATION DISCLOSURE STATEMENT

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Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with the duty of disclosure provisions of 37 CFR §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the subject application.

1. Enclosures accompanying this Information Disclosure Statement are:

   1a. [X] Form PTO-1449.

   1b. [X] Copies of IDS citations.

   1c. [ ] An English language copy of a Search Report or Official Action from a counterpart foreign application or the PCT International Search Report.

   1d. [X] English language translation (complete or relevant portion(s)) attached to each non-English language publication.

   1e. [X] Explanations of Relevancy of References (ATTACHMENT 1(e), hereto) for providing a concise explanation of each non-English publication.

   1f. [ ] List of Copending Applications (ATTACHMENT 1(f), hereto).

2. [X] In accordance with 37 CFR §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

   (Check appropriate Items 2a, 2b, 2c and/or 2d)

   2a. [ ] satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office. (See U.S. Patent & Trademark Office's authorization in the Federal Register, Vol. 57, No. 12, January 17, 1992, at page 2031 (Reply to Comment 68).)

   2b. [ ] set forth in the application.

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2c. [X] satisfied because an English language translation (complete or relevant portion(s)) is attached to each non-English language publication.

2d. [X] enclosed as Attachment 1(e), hereto.

3. No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than search report(s) from a counterpart foreign application or a PCT International Search Report, if submitted herewith). 37 CFR §§ 1.97(g) and (h).

Respectfully submitted,

STAAS & HALSEY LLP

Dated: September 28, 2000

By: _____

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ATTACHMENT 1(e)

EXPLANATIONS OF RELEVANCY OF REFERENCES	ATTORNEY DOCKET NO. 1614.1082	APPLICATION NO.
	FIRST NAMED INVENTOR Hideo MIYAKE et al.	
	FILING DATE September 28, 2000	GROUP ART UNIT

Reference AG discloses a semiconductor memory in which a random access memory (RAM) area is set for an arbitrary entry inside an arbitrary area of a cache memory. This shows a background technology of the present invention.

Reference AG discloses a data storage device which is provided in a data processor and can be used by the data processor as a cache memory or as a random access memory (RAM). This shows a background technology of the present invention.

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INFORMATION DISCLOSURE STATEMENT w/FORM PTO-1449 AND REFERENCES

APPLICANT(S):	Hideo MIYAKE et al.
SERIAL NO:	09/671,117
CONFIRMATION NO.	8617
TITLE:	METHOD OF CONTROLLING A CACHE MEMORY TO INCREASE AN ACCESS SPEED TO A MAIN MEMORY, AND A COMPUTER USING THE METHOD
FILING DATE:	September 28, 2000
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